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ACF12-02-V1.1

Halow WIFI

DESIGNED	Xiaowuxiong
REVISER	
REV	V1_1

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CHANGE LIST

Revision History

REV. CODE	DATE	Description
V1_0	2024/12/11	New Design
V1_1	2025/04/11	1. Increase the terminal resistance for SPI communication, and increase the RC loop for CLK 2. The GPIOs of the halow module are connected to 10K to the ground to avoid floating, which will cause variable power loss. 3. Supplier feedback that R5 will not be welded

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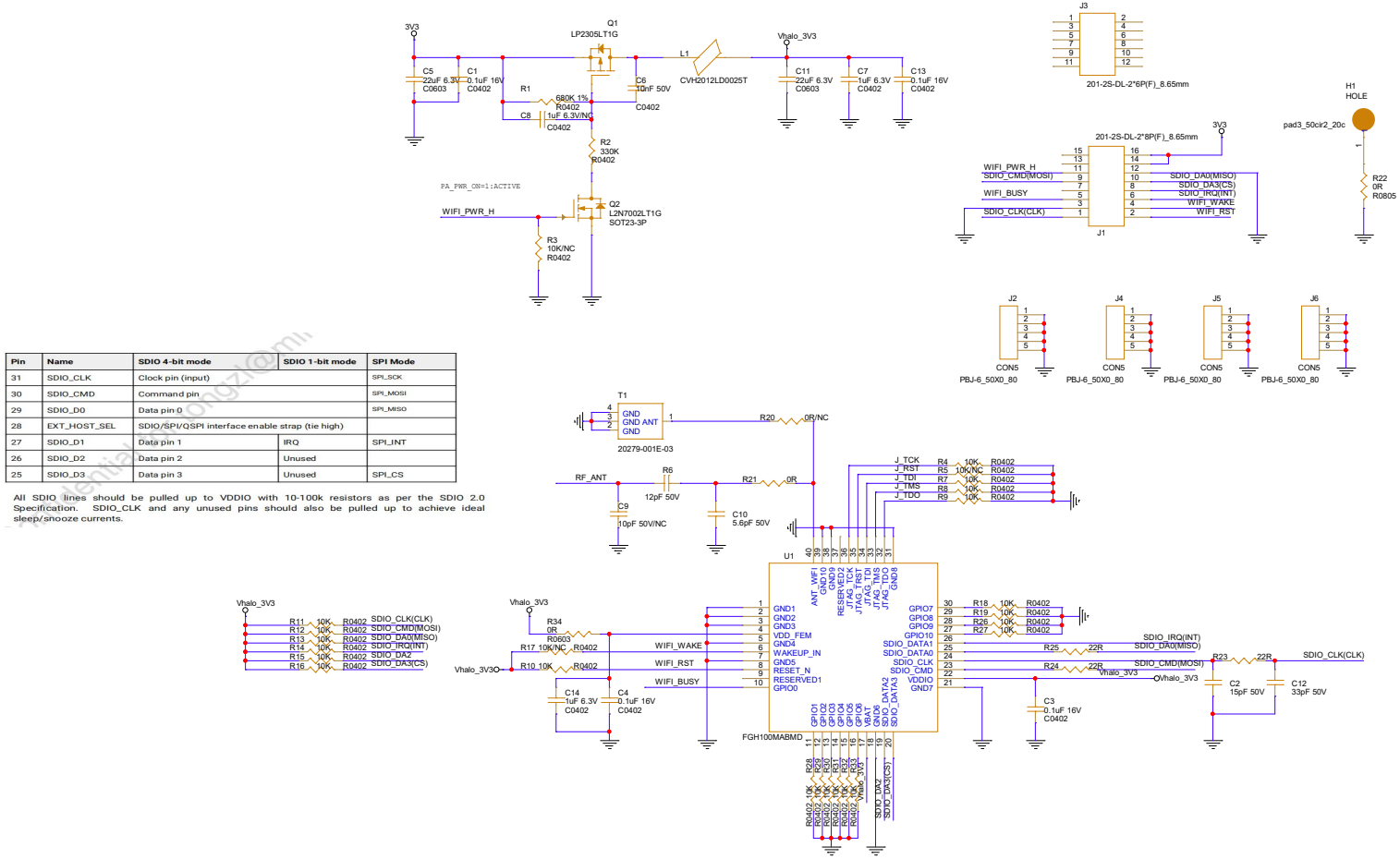
Halow WIFI



Pin	Name	SDIO 4-bit mode	SDIO 1-bit mode	SPI Mode
31	SDIO_CLK	Clock pin (input)		SPI_SCK
30	SDIO_CMD	Command pin		SPI_MOSI
29	SDIO_D0	Data pin 0		SPI_MISO
28	EXT_HOST_SEL	SDIO/SPI/QSPI interface enable strap (tie high)		
27	SDIO_D1	Data pin 1	IRQ	SPI_INT
26	SDIO_D2	Data pin 2	Unused	
25	SDIO_D3	Data pin 3	Unused	SPI_CS

All SDIO lines should be pulled up to VDDIO with 10-100k resistors as per the SDIO 2.0 Specification. SDIO_CLK and any unused pins should also be pulled up to achieve ideal sleep/snooze currents.

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